



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/451,915	12/01/1999	RYUJI NISHIMURA	H-864	9658

24956 7590 07/07/2005

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.  
1800 DIAGONAL ROAD  
SUITE 370  
ALEXANDRIA, VA 22314

EXAMINER

YE, LIN

ART UNIT	PAPER NUMBER
----------	--------------

2615

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/451,915	<b>Applicant(s)</b> NISHIMURA ET AL.	
	<b>Examiner</b> Lin Ye	<b>Art Unit</b> 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 April 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-20 filed on 4/28/05 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, in view of Suzuki et al. U.S. Patent 5,786,852, in view of Parulski et al. U. S. Patent 5,668,597, and further in view of Kato, U.S. Patent 6,148,031.

Regarding claim 1, the admitted prior art teaches cameras that are able to pick up both still and motion images (page 1, lines 14-15). The admitted prior art teaches an image pickup device (page 1, line 5) comprising: a photoelectric sensor (CCD), wherein the pixel signals accumulated in each pixels are outputted with interlace by subsampling the pixel signals for every one line when capturing a still image, which reads on a first signal read mode (page 2, lines 2-7). It is an inherent feature of a CCD to have pixels arranged in the vertical and horizontal directions for converting the light focused on the pixels to electric pixel signals. The admitted Prior art teaches that for a still image, pixel signals of odd number lines are

read on the first field, pixel signals of even number lines are read on the second field, and the still image is generated by sequentially converting the signals of the first and second fields, which reads on an interlace/non-interlace converter for converting the signals with the interlace, which output from the photoelectric sensor in the first signal read mode, to a non-interlaced signal (page 2, lines 5-9).

The admitted prior art does not teach that a sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in a second signal read mode.

The Suzuki reference teaches in Figure 7A, an image pickup device comprising: a photoelectric sensor having pixels arranged in the vertical and horizontal directions for converting light focused on the pixels to electric pixel signals, the pixel signals accumulated in each of the pixels are outputted with interlace by subsampling the pixel signals for every one line in a first signal read mode (e.g., a frame reading mode as the first signal read mode, signals of pixels **with interlace** on odd numbered lines and those on even numbered lines are transferred **separately** to the vertical transfer part, see Col. 1, lines 37-40), and a sum of the pixel signals in the sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in a second signal read mode (e.g., a field reading mode as the second signal read mode, signals of **all pixels** are acquired into the vertical transfer part signals of two pixels adjacent in the vertical direction are added together— this is considered as the signals output with **non-interlace** in this mode). The Suzuki reference is evidenced that one of ordinary skill in the art at time time to see more advantages for driving CCD has more flexible methods, such as read signals of pixels **with**

Art Unit: 2615

**interlace** on odd numbered lines and those on even numbered lines are transferred **separately** to the vertical transfer part in the first reading mode; and sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in the second reading mode, so that the image pickup device be able to generate retain resolution for high-quality still images and improve temporal scalability and sensitivity for moving images with fast scanning in solid state imaging device. For that reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in the second signal read mode taught by Suzuki.

The admitted prior art does not explicitly disclose a signal processor for converting signals in a specified format, or a rate converter for converting the number of the video (moving) signals into another number which is more than the number of output images before conversion, from a non-interlaced scan into an interlaced scan, and converts a number of lines of the output images of the video signal into another number which is less than the number of lines before the conversion and which is approximately equal to the number of lines of a field displayed on a monitor, wherein the monitor displays plural fields with interlace.

The Parulski reference teaches in Figures 1 and 10, an image pickup device comprising a predetermined processor for converting the **noninterlaced** scan signals output by the photoelectric sensor (20 see Col. 4, lines 66-67) to a standard television signals (NTSC, e.g, It is well known the NTSC are **interlace** scan signals, see also Applicants's admitted prior

art page 1, line 27). The Parulski reference discloses the noninterlaced scan signals output from the image sensor at the rate of one picture per 1/30 seconds which is twice slower than NTSC video rates; the NTSC video rates require at the rate of one picture per 1/60 seconds; and the prior art of Parulski reference increase the image sensor readout clock rate of approximately twice that used with the interlaced image sensor; however, high clock rate requires more expensive clock drivers, analog processing, and A/D conversion than interlaced sensors require (See Col. 2, lines 32-55 and Col. 6, lines 52-60). Regarding this situation, the Parulski reference discloses a new improved image pickup device comprising a rate converter (e.g., the fast dump structure 62, see Col. 5, lines 47-53) which converting the number of the video (moving) signals into another number which is more than the number of output images before conversion, from a non-interlaced scan into an interlaced scan, and converts a number of lines of the output images of the video signal into another number which is less than the number of lines before the conversion and which is approximately equal to the number of lines of a field displayed on a monitor, wherein the monitor displays plural fields with interlace (e.g., because dropping or eliminating some lines of image signals readout from image sensor, more "images" updates can be obtained in a given period of times, and lines of output images is less than the number of lines original image signal which is approximately equal to the number of lines of a field displayed on a NTSC interlace monitor, see Col. 6, lines 1-30). The Parulski reference is evidenced that one of ordinary skill in the art at the time to see more advantages for the image sensor device including the rate converter (fast dump structure 62) as mentioned above so that significantly reducing the cost of operation of image sensor and the autofocus can be achieved more rapidly. For that

reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image pickup device of applicant's admitted prior art for providing a signal processor for converting signals in a specified format, or a rate converter for converting the number of the video (moving) signals into another number which is more than the number of output images before conversion, from a non-interlaced scan into an interlaced scan, and converts a number of lines of the output images of the video signal into another number which is less than the number of lines before the conversion and which is approximately equal to the number of lines of a field displayed on a monitor, wherein the monitor displays plural fields with interlace as taught by Parulski.

The admitted prior art also does not teach an encoder for compressing the signals from the signal processor, a memory device, or a decoder.

The Kato reference teaches an encoder (image compression/decompression circuit 18) for generating a first or second image data by compressing the first or second signals output from the signal processor (digital signal processor circuit 14) (col. 3, lines 42-53); a memory device (first memory 20) for memorizing the first or second image data output from the encoder (image compression/decompression circuit 18) (col. 3, lines 46-47, 50-53); and a decoder (image compression/decompression circuit 18) for reproducing the first signal by decoding the first image data memorized in the memory device (first memory 20) (col. 5, lines 23-29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interlace/non-interlace reading methods of the admitted prior art in view of Suzuki and Nobuoka with the compression/decompression units of Kato to make an image sensing apparatus that reads still and motion images using the

same image pickup device, and processes, encodes, stores, and decodes the data. One of ordinary skill would have been motivated to make such a modification to enable a camera to process both still and motion images so as to minimize the amount of memory required to store the images.

Regarding claim 2, the admitted prior does not explicitly teach that said interlace/non-interlace converter and said rate converter comprises a memory for storing said signals output from the photoelectric sensor, and a memory controller for controlling writing and reading addresses and timings.

The Parulski reference teaches in Figure 1, the memory (DRAM memory 38) for storing the signals output from the photoelectric sensor, and a memory controller (controller 52) for controlling writing and reading addresses and timings (See Col. 4, lines 31-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by the admitted prior art with the practice of storing and reading out signals taught by Parulski to make an apparatus that stores signals in a predetermined fashion and reads out the signals in order to save for processing later. One of ordinary skill would have been motivated to make such a modification to achieve a slower clock rate while reproducing entire images.

Regarding claim 3, the admitted prior art teaches that the first signal generated in the first signal read mode is a still image (page 2, line 2), and the second signal generated in the second signal read mode is a motion image signal (page 1, line 25).



Regarding claim 4, the admitted prior art teaches that the effective pixel number of said photoelectric sensor in vertical direction approximates multiplication by an integer of the effective number of scanning lines in the television signal standard (page 2, lines 15-17).

Regarding claim 5, Kato teaches that individual images may be tagged as still images, which reads on the first image data representing one still image, and that the images captured during continuous image taking are a series of still images (col. 3, lines 47-56).

Regarding claim 6, the admitted prior art teaches that said arrangement of said pixels on said photoelectric sensor has a cycle of a units of two rows in the vertical direction and four lines in the horizontal direction, the pixels of the first color and the pixels of the second color are arranged alternately in the first lines, the pixels of the third color and the pixels of the fourth color are arranged alternately in the second lines, the pixels of the second color and the pixels of the first color are arranged alternately in the third lines, and the pixels of the third color and the pixels of the fourth color are arranged alternately in the fourth lines (page 1, line 20-23; Fig. 3A).

Regarding claim 7, the admitted prior art teaches that said first color is magenta, said second color is green, said third color is cyan, and said fourth color is yellow (Fig. 3A).

Regarding claim 8, the Parulski reference teaches the use of green, blue, and red as the colors in the color filter (See Figure 3). It would have been obvious to one of ordinary skill to substitute the green, blue, and red colors into the filter arrangement of claim 6.

Regarding claim 9, the admitted prior art teaches that the effective pixel number of said photoelectric sensor in vertical direction approximates multiplication by an integer of the effective number of scanning lines in the television signal standard (page 2, lines 15-17).

Regarding claim 10, the admitted prior art teaches that the effective pixel number of said photoelectric sensor is 960, which is between 920 and 1020 (page 2, line 16).

Regarding claim 11, the admitted prior art teaches cameras that are able to pick up both still and motion images (page I, lines 14-15). The admitted prior art teaches an image pickup device (page 1, line 5) comprising: a photoelectric sensor (CCD), wherein the pixel signals accumulated in each pixels are outputted with interlace by subsampling the pixel signals for every one line when capturing a still image, which reads on a first signal read mode (page 2, lines 2-7). It is an inherent feature of a CCD to have pixels arranged in the vertical and horizontal directions for converting the light focused on the pixels to electric pixel signals. The admitted Prior art teaches that for a still image, pixel signals of odd number lines are read on the first field, pixel signals of even number lines are read on the second field, and the still image is generated by sequentially converting the signals of the first and second fields, which reads on an interlace/non-interlace converter for converting the signals with the interlace, which output from the photoelectric sensor in the first signal read mode, to a non-interlaced signal (page 2, lines 5-9).

The admitted prior art does not teach that a sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in a second signal read mode.

The Suzuki reference teaches in Figure 7A, an image pickup device comprising: a photoelectric sensor having pixels arranged in the vertical and horizontal directions for converting light focused on the pixels to electric pixel signals, the pixel signals accumulated in each of the pixels are outputted with interlace by subsampling the pixel signals for every

Art Unit: 2615

one line in a first signal read mode (e.g., a frame reading mode as the first signal read mode, signals of pixels **with interlace** on odd numbered lines and those on even numbered lines are transferred **separately** to the vertical transfer part, see Col. 1, lines 37-40), and a sum of the pixel signals in the sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in a second signal read mode (e.g., a field reading mode as the second signal read mode, signals of **all pixels** are acquired into the vertical transfer part signals of two pixels adjacent in the vertical direction are added together— this is considered as the signals output with **non-interlace** in this mode). The Suzuki reference is evidenced that one of ordinary skill in the art at time time to see more advantages for driving CCD has more flexible methods, such as read signals of pixels **with interlace** on odd numbered lines and those on even numbered lines are transferred **separately** to the vertical transfer part in the first reading mode; and sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in the second reading mode, so that the image pickup device be able to generate retain resolution for high-quality still images and improve temporal scalability and sensitivity for moving images with fast scanning in solid state imaging device. For that reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the sum of the pixel signals in the two pixels adjoining each other in the vertical direction are sequentially outputted with **non-interlace** in the second signal read mode taught by Suzuki.

The admitted prior art does not explicitly disclose a signal processor for converting signals in a specified format, or a rate converter for converting the number of the video

(moving) signals into another number which is more than the number of output images before conversion, from a non-interlaced scan into an interlaced scan, and converts a number of lines of the output images of the video signal into another number which is less than the number of lines before the conversion and which is approximately equal to the number of lines of a field displayed on a monitor, wherein the monitor displays plural fields with interlace.

The Parulski reference teaches in Figures 1 and 10, an image pickup device comprising a predetermined processor for converting the **noninterlaced** scan signals output by the photoelectric sensor (20 see Col. 4, lines 66-67) to a standard television signals (NTSC, e.g., It is well known the NTSC are **interlace** scan signals, see also Applicants's admitted prior art page 1, line 27). The Parulski reference discloses the noninterlaced scan signals output from the image sensor at the rate of one picture per 1/30 seconds which twice slower than NTSC video rates; the NTSC video rates require at the rate of one picture per 1/60 seconds; and the prior art of Parulski reference increase the image sensor readout clock rate of approximately twice that used with the interlaced image sensor; however, high clock rate requires more expensive clock drivers, analog processing , and A/D conversion than interlaced sensors require (See Col. 2, lines 32-55 and Col. 6, lines 52-60). Regarding this situation, the Parulski reference discloses a new improved image pickup device comprising a rate converter (e.g., the fast dump structure 62, see Col. 5, lines 47-53) which converting the number of the video (moving) signals into another number which is more than the number of output images before conversion, from a non-interlaced scan into an interlaced scan, and converts a number of lines of the output images of the video signal into another number

which is less than the number of lines before the conversion and which is approximately equal to the number of lines of a field displayed on a monitor, wherein the monitor displays plural fields with interlace (e.g., because dropping or eliminating some lines of image signals readout from image sensor, more "images" updates can be obtained in a given period of times, and lines of output images is less than the number of lines original image signal which is approximately equal to the number of lines of a field displayed on a NTSC interlace monitor, see Col. 6, lines 1-30). The Parulski reference is evidenced that one of ordinary skill in the art at time time to see more advantages for the image sensor device including the rater converter (fast dump structure 62) as mentioned above so that significantly reducing the cost of operation of image sensor and the autofocus can be achieved more rapidly. For that reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image pickup device of applicant's admitted prior art for providing a signal processor for converting signals in a specified format, or a rate converter for converting the number of the video (moving) signals into another number which is more than the number of output images before conversion, from a non-interlaced scan into an interlaced scan, and converts a number of lines of the output images of the video signal into another number which is less than the number of lines before the conversion and which is approximately equal to the number of lines of a field displayed on a monitor, wherein the monitor displays plural fields with interlace as taught by Parulski.

The admitted prior art also does not teach an encoder for compressing the signals from the signal processor, a memory device, or a decoder.

The Kato reference teaches an encoder (image compression/decompression circuit 18) for generating a first or second image data by compressing the first or second signals output from the signal processor (digital signal processor circuit 14) (col. 3, lines 42-53); a memory device (first memory 20) for memorizing the first or second image data output from the encoder (image compression/decompression circuit 18) (col. 3, lines 46-47, 50-53); and a decoder (image compression/decompression circuit 18) for reproducing the first signal by decoding the first image data memorized in the memory device (first memory 20) (col. 5, lines 23-29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interlace/non-interlace reading methods of the admitted prior art in view of Suzuki and Nobuoka with the compression/decompression units of Kato to make an image sensing apparatus that reads still and motion images using the same image pickup device, and processes, encodes, stores, and decodes the data. One of ordinary skill would have been motivated to make such a modification to enable a camera to process both still and motion images so as to minimize the amount of memory required to store the images.

Regarding claim <sup>13</sup>~~2~~, the admitted prior does not explicitly teach that said interlace/non-interlace converter and said rate converter comprises a memory for storing said signals output from the photoelectric sensor, and a memory controller for controlling writing and reading addresses and timings.

The Parulski reference teaches in Figure1, the memory (DRAM memory 38) for storing the signals output from the photoelectric sensor, and a memory controller (controller 52) for controlling writing and reading addresses and timings (See Col. 4, lines 31-45). Therefore, it

6/30/05

would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by the admitted prior art with the practice of storing and reading out signals taught by Parulski to make an apparatus that stores signals in a predetermined fashion and reads out the signals in order to save for processing later. One of ordinary skill would have been motivated to make such a modification to achieve a slower clock rate while reproducing entire images.

Regarding claims 13, the admitted prior art teaches that the first signal generated in the first signal read mode is a still image (page 2, line 2), and the second signal generated in the second signal read mode is a motion image signal (page 1, line 25).

Regarding claim 14, the admitted prior art teaches that the effective pixel number of said photoelectric sensor in vertical direction approximates multiplication by an integer of the effective number of scanning lines in the television signal standard (page 2, lines 15-17).

Regarding claim 15, Kato teaches that individual images may be tagged as still images, which reads on the first image data representing one still image, and that the images captured during continuous image taking are a series of still images (col. 3, lines 47-56).

Regarding claim 16, the admitted prior art teaches that said arrangement of said pixels on said photoelectric sensor has a cycle of a units of two rows in the vertical direction and four lines in the horizontal direction, the pixels of the first color and the pixels of the second color are arranged alternately in the first lines, the pixels of the third color and the pixels of the fourth color are arranged alternately in the second lines, the pixels of the second color and the pixels of the first color are arranged alternately in the third lines, and the pixels of the

third color and the pixels of the fourth color are arranged alternately in the fourth lines (page 1, line 20-23; Fig. 3A).

Regarding claim 17, the admitted prior art teaches that said first color is magenta, said second color is green, said third color is cyan, and said fourth color is yellow (Fig. 3A).

Regarding claim 18, the Parulski reference teaches the use of green, blue, and red as the colors in the color filter (page 2, lines 17-20; Fig. 3C). It would have been obvious to one of ordinary skill to substitute the green, blue, and red colors into the filter arrangement of claim 6.

Regarding claim 19, the admitted prior art teaches that the effective pixel number of said photoelectric sensor in vertical direction approximates multiplication by an integer of the effective number of scanning lines in the television signal standard (page 2, lines 15-17).

Regarding claims 20, the admitted prior art teaches that the effective pixel number of said photoelectric sensor is 960, which is between 920 and 1020 (page 2, line 16).

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
  - a. Hayashi U.S. Patent 5,734,427 discloses an electronic camera outputs image signal to an NTSC monitor in a lower resolution mode.



Art Unit: 2615

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lin Ye whose telephone number is (571) 272-7372. The examiner can normally be reached on Mon-Fri 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2615

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DAVID L. OMETZ  
PRIMARY EXAMINER

Lin Ye

June 24, 2005